IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

James Herbert Kukula et al.

Appl. No. 10/046,220

Filed: January 16, 2002

METHOD AND APPARATUS FOR FORMALLY CONSTRAINING

RANDOM SIMULATION

Conf. No. 4032

Art Unit: 2185

Examiner: TBD

Atty. Docket: 06816.0110

Cust. No. 35795

Information Disclosure Statement

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Sir:

The Examiner is requested to consider the documents listed on accompanying Form PTO/SB/08B and make this information of official record in the application.

Applicants have listed publication dates on the attached PTO/SB/08B based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right, with respect to any of the information provided herewith, to prove that this information may not be prior art and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

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Applicants Kukula et al. Appl. No. 10/046,220

- ☑ 1. This Information Disclosure Statement is being filed within three months of the
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It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO/SB/08B, and to indicate in the official file wrapper of this patent application that the documents have been considered.

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Applicants Kukula et al. Appl. No. 10/046,220

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 502584 referencing docket number 06816.0110.

Respectfully submitted,

Jonathan T. Kaplan (Reg. No. 38,935)

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Date: Mar. 6, 2004
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PTO/SB/08B (08-03)

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Substituti	e lot totili 1443F 10			Application Number	10/046,220	
INFORMATION DISCLOSURE				Filing Date	January 16, 2002	
STATEMENT BY APPLICANT			PPLICANT	First Named Inventor	James Herbert Kukula	
(Use as many sheets as necessary)				Art Unit	2185	
				Examiner Name		
Sheet	1	of	1	Attorney Docket Number	06816.0110	

		NON PATENT LITERATURE DOCUMENTS		
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
	1	H. Cho, G. D. Hachtel, E. Macii, B. Plessier, and F. Somenzi. "Algorithms for Approximate FSM Traversal." Proc. 30th ACM/IEEE Design Automation Conference, pp. 25-30, 1993.		
	2	H. Cho, G. D. Hachtel, E. Macii, M. Poncino, and F. Somenzi. *A Structural Approach to State Space Decomposition for Approximate Reachability Analysis.* In Proc. IEEE Intl. Conf. on Computer Design (ICCD), October 10-12, 1994, pp236-239.		
	3	H. Cho, G. D. Hachtel, E. Macii, M. Poncino, and F. Somenzi. *Automatic State Space Decomposition for Approximate FSM Traversal Based on Circuit Analysis.* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, No. 12, December 1996, pp1451-1464.		
	4	H. Cho, G. D. Hachtel, E. Macli, B. Plessier, and F. Somenzi. "Algorithms for Approximate FSM Traversal Based on State Space Decomposition." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, No. 12, December 1996, pp1465-1478.		
	5	C. H. Yang and D. L. Dill. "Validation with Guided Search of the State Space." In Proc. of the Design Automation Conf., June 1998, pp599-604.		
•	6	Govindaraju, G. S. and Dill, D. L. "Verification by Approximate Forward and Backward Reachability." IEEE/ACM ICCAD, pp. 366-370, Nov. 8-12, 1998.		

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